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In fetch operation the microprocessor gets the 1st byte of the instruction, which is operation code (opcode), from the memory. The program counter keeps the track of address of the next instruction to be executed. In the beginning of the fetch cycle the content of the program counter is sent to the memory. This takes one clock cycle. The memory first reads the opcode. This operation also takes one clock cycle. Then the memory sends the opcode to the microprocessor, which takes one clock period. The total time for fetch operation is the time required for fetching an opcode from the memory. This time is called fetch cycle. Having received the address from the microprocessor the memory takes two clock cycles to respond as explained above. If the memory is slow, it may take more time. In that case the microprocessor has to wait for some time till it receives the opcode from the memory. The time for which the microprocessor waits is called wait cycle. Most of the microprocessor have provision for wait cycles to cope with slow memory.

# **Execute Operation**

The opcode fetched from the memory goes to the data register, DR (data/address buffer in Intel 8085) and then to instruction register, IR. From the instruction register it goes to the decoder circuitry is within the microprocessor. After the instruction is decoded, execution begins. If the operand is in the general purpose registers, execution is immediately performed. The time taken in decoding and the address of the data, some read cycles are also necessary to receive the data from the memory. These read cycle are similar to opcode fetch cycle. The fetch quantities in these cycles are address or data. Figure 4 (a) and Figure 4 (b) shows an instruction and fetch cycle respectively.

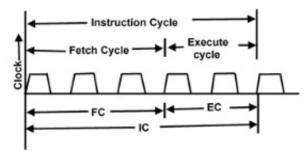
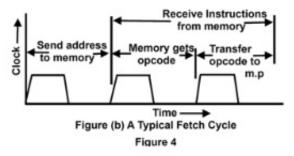


Figure (a) Instruction cycle showing FC, EC and IC



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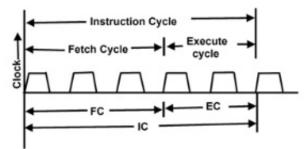
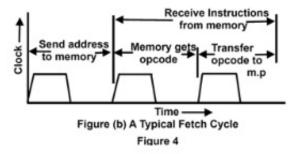


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